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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/001,791	12/05/2001	Toshimitsu Tamagawa	103213-00042	2283

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EXAMINER

JELINEK, BRIAN J

ART UNIT	PAPER NUMBER
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2615

DATE MAILED: 09/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/001,791

Applicant(s)

TAMAGAWA, TOSHIMITSU

Examiner

Brian Jelinek

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 December 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-8 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 05 December 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This is a first office action in response to application no. 10/001,791 filed on 12/5/2001 in which claims 1-8 are presented for examination.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, and 4-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita (U.S. Pat. No. 5,268,765).

Regarding claim 1, Yamashita discloses an IC chip (Fig. 3, sensor chips 15-1, 15-2, and 15-3) for reading an image, comprising: a plurality of image reading photoelectric conversion elements (Fig. 8, photocells 1-1 to 1-N); a plurality of first transistors for reading a first photoelectric conversion signal from the image reading photoelectric conversion elements (Fig. 8, channel select switches 4-1 to 4-N); a first signal selection circuit for sequentially selecting the plurality of first transistors (Fig. 8, shift register 5 for performing successive closures of the channel select switches 4-1 to 4-N); a plurality of dummy photoelectric conversion elements arranged respectively near the image reading photoelectric conversion elements and shielded from light (Fig. 8, dummy photocell 16, one dummy photocell per sensor chip 15-1 to 15-N); and a

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plurality of second transistors for reading a second photoelectric conversion signal from the dummy photoelectric conversion elements (Fig. 8, dummy select switch 17, one dummy select switch per sensor chip 15-1 to 15-N); a second signal selection circuit for sequentially selecting the plurality of second transistors (Fig. 8, dummy select switch 4-N).

Furthermore, Yamashita discloses a signal line 3 for outputting the photocell and dummy photocell signal; and the dummy photocell outputs a reference level for the dark output. Yamashita does not disclose an output circuit for processing the first and second photoelectric conversion signals and then outputting a resulting signal, wherein the output circuit outputs a difference between the first and second photoelectric conversion signals to correct the first photoelectric conversion signal. However, Official Notice is given that one of ordinary skill in the art would have outputted the difference between the photocell signal and dummy photocell signal since this is the value of the light signal because the photocell signal is a sum of the dark current and the light signal. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to have provided an output circuit for processing the first and second photoelectric conversion signals and then outputting a resulting signal, wherein the output circuit outputs a difference between the first and second photoelectric conversion signals to correct the first photoelectric conversion signal since this is the value of the light signal because the photocell signal is a sum of the dark current and the light signal.

Regarding claim 4, Yamashita discloses an IC chip (Fig. 3, sensor chips 15-1, 15-2, and 15-3) for reading an image, comprising: a plurality of first processing sections,

each comprising: a plurality of image reading photoelectric conversion elements (Fig. 8, photocells 1-1 to 1-N); a plurality of first transistors for reading a first photoelectric conversion signal from the image reading photoelectric conversion elements (Fig. 8, channel select switches 4-1 to 4-N); a first signal selection circuit for sequentially selecting the plurality of first transistors (Fig. 8, shift register 5 for performing successive closures of the channel select switches 4-1 to 4-N); and a first signal output line by way of which the first photoelectric conversion signal is transmitted (Fig. 8, signal line 3); a plurality of second processing sections provided so as to pair respectively with the first processing sections, the second processing sections each comprising: a plurality of dummy photoelectric conversion elements arranged respectively near the image reading photoelectric conversion elements and shielded from light (Fig. 8, dummy photocell 16, one dummy photocell per sensor chip 15-1 to 15-N); a plurality of second transistors for reading a second photoelectric conversion signal from the dummy photoelectric conversion elements (Fig. 8, dummy select switch 17, one dummy select switch per sensor chip 15-1 to 15-N); a second signal selection circuit for sequentially selecting the plurality of second transistors (Fig. 8, dummy select switch 4-N); and a second signal output line by way of which the second photoelectric conversion signal is transmitted (Fig. 8, signal line 3, wherein the first and second output lines are the same).

Furthermore, Yamashita discloses a signal line 3 for outputting the photocell and dummy photocell signal; and the dummy photocell outputs a reference level for the dark output. Yamashita does not disclose an output circuit for processing the first and

second photoelectric conversion signals and then outputting a resulting signal; and a signal output line switching circuit for selecting the first and second signal output lines and connecting the selected first and second signal output lines to the output circuit, wherein the output circuit outputs a difference between the first and second photoelectric conversion signals to correct the first photoelectric conversion signal.

However, Official Notice is given that one of ordinary skill in the art would have outputted the difference between the photocell signal and dummy photocell signal since this is the value of the light signal because the photocell signal is a sum of the dark current and the light signal. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to have provided an output circuit for processing the first and second photoelectric conversion signals and then outputting a resulting signal; and a signal output line switching circuit for selecting the first and second signal output lines and connecting the selected first and second signal output lines to the output circuit, wherein the output circuit outputs a difference between the first and second photoelectric conversion signals to correct the first photoelectric conversion signal since this is the value of the light signal because the photocell signal is a sum of the dark current and the light signal.

Regarding claim 5, please see the rejection of claim 1. Yamashita further discloses a trigger signal input terminal by way of which a signal for sequentially scanning an image being read is fed in from an IC chip in a previous stage (Fig. 8, start pulse SI 6); a trigger signal output terminal by way of which a signal for sequentially scanning the image being read is fed out to an IC chip in a following stage (Fig. 8,

element SO 9); a clock input terminal by way of which a clock is fed in (Fig. 8, CLK 7); and a reference voltage input terminal by way of which a reference voltage for the output circuit is fed in (Fig. 8, VDD 2); and an A/D converter for converting a signal output from the output circuit into a digital signal (implicit in the overall teaching of the reference), wherein said one or more IC chips each start scanning the image being read on receiving an input signal at the trigger input terminal thereof, and, on completion of the scanning, outputs, at the trigger output terminal thereof, a signal for continuing sequential scanning to the IC chip in the following stage.

Regarding claim 6, please see the rejection of claim 5.

Regarding claim 7, please see the rejection of claim 5.

Regarding claim 8, please see the rejection of claim 4. Yamashita further discloses a trigger signal input terminal by way of which a signal for sequentially scanning an image being read is fed in from an IC chip in a previous stage (Fig. 8, start pulse SI 6); and a trigger signal output terminal by way of which a signal for sequentially scanning the image being read is fed out to an IC chip in a following stage (Fig. 8, element SO 9); a clock input terminal by way of which a clock is fed in (Fig. 8, CLK 7); and an A/D converter for converting a signal output from the output circuit into a digital signal (implicit in the overall teaching of the reference), wherein said one or more IC chips each start scanning the image being read on receiving an input signal at the trigger input terminal thereof, and, on completion of the scanning, outputs, at the trigger output terminal thereof, a signal for continuing sequential scanning to the IC chip in the following stage.

Claims 2-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita (U.S. Pat. No. 5,268,765) in view of Aswell et al. (U.S. Pat. No. 6,553,437).

Regarding claim 2, Yamashita discloses an IC chip (Fig. 3, sensor chips 15-1, 15-2, and 15-3) for reading an image, comprising: a plurality of first processing sections, each comprising: a plurality of image reading photoelectric conversion elements (Fig. 8, photocells 1-1 to 1-N); a plurality of first transistors for reading a first photoelectric conversion signal from the image reading photoelectric conversion elements (Fig. 8, channel select switches 4-1 to 4-N); a first signal selection circuit for sequentially selecting the plurality of first transistors (Fig. 8, shift register 5 for performing successive closures of the channel select switches 4-1 to 4-N); and a first signal output line by way of which the first photoelectric conversion signal is transmitted (Fig. 8, signal line 3).

Furthermore, Yamashita discloses connecting the signal outputs of each sensor chip to a common bus (Fig. 3, SIG terminal 31). Yamashita does not disclose a provision of the plurality of first processing sections reduces a total resistance and a total capacitance of the first signal output lines provided within the first processing sections, reduces a total parasitic capacitance of the first transistors connected to the first signal output lines, and thereby permits the image reading device to operate at a higher operation speed.

However, Aswell discloses an IC chip (Fig. 1) comprising sensor chips (Device 1 to Device n), wherein the signal outputs of each sensor device are outputted to a common signal line (Fig. 1, element 100), and alternatively, wherein the signal outputs

of each sensor device are outputted in parallel (Fig. 4). One of ordinary skill in the art would have outputted the signals of the sensor devices in parallel, rather than on a common signal line, in order to provide the signal outputs of each sensor device directly to a controller (col. 5, lines 13-17). As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to have outputted the signals of the sensor devices in parallel, rather than on a common signal line, in order to provide the signal outputs of each sensor device directly to a controller.

Furthermore, it is implicit that a provision of the plurality of first processing sections reduces a total resistance and a total capacitance of the first signal output lines provided within the first processing sections, reduces a total parasitic capacitance of the first transistors connected to the first signal output lines, and thereby permits the image reading device to operate at a higher operation speed because when the sensor devices are configured to output signals in parallel to a controller, the individual bus lines are shorter than the common bus (informally, compare the length of bus 100 in Fig. 1 to the length of the individual bus lines in Fig. 4); and consequently, since the bus line is shorter, the resistance and capacitance of the bus is less.

Regarding claim 3, Yamashita further discloses a dummy photoelectric conversion element shielded from light (Fig. 8, dummy photocell 16, one dummy photocell per sensor chip 15-1 to 15-N).

Furthermore, Yamashita discloses a signal line 3 for outputting the photocell and dummy photocell signal; and the dummy photocell outputs a reference level for the dark output. Yamashita does not disclose output circuit for outputting a difference between

the first photoelectric conversion signal and a second photoelectric conversion signal read from the dummy photoelectric conversion element, wherein the output circuit corrects the first photoelectric conversion signal. However, Official Notice is given that one of ordinary skill in the art would have outputted the difference between the photocell signal and dummy photocell signal since this is the value of the light signal because the photocell signal is a sum of the dark current and the light signal. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to have provided an output circuit for outputting a difference between the first photoelectric conversion signal and a second photoelectric conversion signal read from the dummy photoelectric conversion element, wherein the output circuit corrects the first photoelectric conversion signal since this is the value of the light signal because the photocell signal is a sum of the dark current and the light signal.


Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Jelinek whose telephone number is (571) 272-7366. The examiner can normally be reached on M-F 9:00 am - 5:00 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached at (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian Jelinek
9/15/2005



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EXAMINER